ABSTRACT

The invention is concerned with a method for producing a chip-scale electronic package produced at the substrate level, with the substrate being made up of at least one chip with this chip having input/output pads on a substrate face known as the front face, with the method involving the following steps:

a) formation, using a complex mould or stencil of an insulating stress relaxation layer on the aforementioned front face, with the aforementioned relaxation layer covering the front face of the substrate with a surface relief which provides access wells at input/output pads and as well as protruding parts intended to relax stresses, with each protruding part having a tiered shape made up of at least one protuberant zone and at least one zone that is recessed in relation to the aforementioned protuberant zone and is intended to support an electrical bonding pad,

b) formation of electrically conductive tracks on the relaxation layer to connect input/output pads to the corresponding electrical bonding pads,

c) formation of means of electrical contact with the exterior on electrical bonding pads.

The invention is also concerned on one hand with a complex mould or stencil used to produce a chip-scale package in accordance with the method in the invention and on the other hand with the aforementioned chip-scale package itself.

No figure.